REMARKS/ARGUMENTS

Claims 1-17 are pending in the application. Claims 1-17 are rejected.

Claims 1-4, 6-12, and 14 are rejected under 35 U.S.C. §102(a) as being unpatentable over Shen et al. U.S. Patent No. 6,526,481 (Hereinafter "Shen"). Claims 5, 13, and 15 are rejected under 35 U.S.C. §103 (a) as being unpatentable over Shen in view of Barroso in further view of Jim Handy, "The Cache Memory Handbook" TK7895.M4H35, 1993, pp. 140-240 (Hereinafter "Handy"). Claims 16-17 are rejected under 35 U.S.C. §103 (a) as being unpatentable over Shen in view of Handy in further view of Witt et al. U.S. Patent No. 6,202,139 (Hereinafter "Witt").

Claim Rejections under 35 U.S.C. §102

Claims 1-4, 6-12, and 14 are rejected under 35 U.S.C. §102(a) as being unpatentable over Shen. Shen discloses a methodology for designing a distributed shared-memory system. The distributed shared-memory system can incorporate adaptation or selection of cache protocols during operation. It guarantees semantically correct processing of memory instructions by the multiple processors. (*See* Abstract).

Applicants respectfully submit that Shen is not a prior art reference under 35 U.S.C. §102(a) as it was not issued as a patent, making it known to the public, until February 25, 2003, long after Applicants' filing date of August 27, 2001. Applicants respectfully submit that Shen does not disclose a cache coherent input/output device. Shen states:

> Referring still to FIG. 2, memory system 120 includes one cache 130 for each instruction processor 110, and shared-memory system 140. Each cache 130 includes a cache controller 132 and a cache storage 134. Cache storage 134 includes data storage which associates address, data, and status information for a limited portion of the address space accessible from instruction processor 110. Cache controller 132 communicates with memory access unit 117. Memory access unit 117 passes memory access messages to

> cache controller 132 in response to memory access instructions issued by instruction pool 114. Cache controller 132 processes these memory access messages by accessing its cache storage 134, by communicating in turn with shared-memory system 140, or both. When it has finished processing a memory access message, it sends a result or acknowledgment back to memory access unit 117, which in turn signals to instruction pool 114 that the corresponding memory access instruction has completed.

(Shen, col. 8, line 45–62).

In other words, Shen describes using cache coherency protocols to allow a number of instruction processors to access a distributed cache memory system. Shen does not describe the use of distributed caches for cache-coherent input/output. The Office Action contends that each storage cache 130 of Shen is a cache coherent input/output device. The storage cache 130 does not disclose the invention of claims 1, 6, and 9, as each semantic cache 130 has only a single port coupled to a single semantic cache storage 134. Further, the Office Action cites the semantic cache controller 132 as the cache coherency engine. Each semantic cache controller 134 is only coupled to a single semantic cache storage 132, rather than to a plurality of cache sub-units as required by the claims. While the memory subsystem 120 as a whole does have multiple ports and cache sub-units, the memory subsystem is not an input/output device, rather it is using multiple semantic caches to connect to multiple instruction processors.

Therefore claims 1, 6, and 9, are not anticipated by Shen. Accordingly reconsideration and withdrawal of the rejection of claims 1, 6, and 9 under 35 U.S.C. §102(a) is respectfully requested. In addition, Applicants respectfully submit that claims 2-4, 7-8, 10-12 and 14 are allowable as depending from allowable base claims 1, 6 and 9.

Claim Rejections under 35 U.S.C. §103

Claims 5, 13, and 15 are rejected under 35 U.S.C. §103 (a) as being unpatentable over Shen in view of Handy. Handy discloses a protocol for use in multiple processor system with

multiple caches.

As discussed above, Shen does not disclose a cache coherent input/output device as recited in claims 1 and 9 as amended, and by their dependency claims 5, 13, and 15. Handy also does not disclose a cache coherent input/output device. Therefore Applicants respectfully submit that claims 5, 13, and 15 are allowable as depending from allowable base claims 1 and 9 given the arguments above.

Claims 16-17 are rejected under 35 U.S.C. §103 (a) as being unpatentable over Shen in view of Handy and in further view of Witt. Witt discloses a pipelined data cache with multiple ports. The invention of Witt is described as a computer system including a processor having a cache that includes multiple ports. The cache is pipelined and operates at a clock frequency higher than that employed by the remainder of the microprocessor including the cache for multiple accesses per clock cycle. (*See* Abstract, Summary of the Invention, col. 2, lines 31-36)

As discussed above, Shen and Handy do not disclose a cache coherent input/output device as recited in claim 9 as amended, and by their dependency claims 16-17. Witt does not disclose a cache coherent input/output device. Therefore Applicants respectfully submit that claims 16-17 are allowable as depending from allowable base claim 9 given the arguments above.

Based on the amendments and arguments above, reconsideration and withdrawal of the rejection of claims 16-17 under 35 U.S.C. §103(a) is respectfully requested.

For all the above reasons, the Applicants respectfully submit that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

The Examiner is invited to contact the undersigned at (408) 975-7500 to discuss any matter concerning this application.

The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. §1.16 or §1.17 to the deposit account of Kenyon & Kenyon, deposit account no. **11-0600**.

Respectfully submitted,

KENYON & KENYON

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